WHAT IS CLAIMED IS:

1. For use in an operational circuit having a high impedance node, a pre-charge circuit capable of pre-charging said high-impedance node to a target voltage when a pre-charge signal driving said pre-charge circuit is enabled, said pre-charge circuit comprising:

a charge voltage circuit capable of charging an internal common node of said pre-charge circuit to said target voltage when said pre-charge signal is enabled;

a transmission gate switch capable of coupling said internal node to said high-impedance node when said pre-charge signal is enabled, said transmission gate switch comprising a first N-channel transistor having a drain coupled to said high-impedance node, a gate coupled to a Logic 1 when said pre-charge signal is enabled, and a source coupled to said internal common node; and

a gate-biasing circuit driven by said pre-charge signal, wherein said gate-biasing circuit is off when said pre-charge signal is enabled and generates a negative Vgs bias on said first N-channel transistor when said pre-charge signal is disabled to thereby reduce leakage current in said first N-channel transistor.

2. The pre-charge circuit as set forth in Claim 1 wherein said transmission gate switch further comprises a first P-channel transistor having a drain coupled to said high-impedance node, a gate coupled to a Logic 0 when said pre-charge signal is enabled, and a source coupled to said internal common node.

3. The pre-charge circuit as set forth in Claim 2 wherein said gate-biasing circuit generates a positive Vgs bias on said first P-channel transistor when said pre-charge signal is disabled to thereby reduce leakage current in said first P-channel transistor.

4. The pre-charge circuit as set forth in Claim 3 wherein said gate of said first N-channel transistor is coupled to a Logic 0 when said pre-charge signal is disabled and said gate-biasing circuit holds said internal common node at a voltage higher than Logic 0 to thereby generate said negative Vgs bias on said first N-channel transistor when said pre-charge signal is disabled.

5. The pre-charge circuit as set forth in Claim 4 wherein said gate of said first P-channel transistor is coupled to a Logic 1 when said pre-charge signal is disabled and said gate-biasing circuit holds said internal common node at a voltage less than Logic 1 to thereby generate said positive Vgs bias on said first P-channel transistor when said pre-charge signal is disabled.

6. The pre-charge circuit as set forth in Claim 5 wherein said charge voltage circuit comprises a first diode-connected transistor and a second diode-connected transistor, wherein said first and second diode-connected transistors are connected as diodes in series between a VDD power supply rail and a ground rail when said pre-charge signal is enabled and wherein said internal common node is a connection node between said first and second diode-connected transistors.

7. The pre-charge circuit as set forth in Claim 6 wherein said target voltage is determined by an impedance of said first diode-connected transistor and an impedance of said second diode-connected transistor when said pre-charge signal is enabled.

8. The pre-charge circuit as set forth in Claim 7 wherein said impedance of said first diode-connected transistor and said impedance of said second diode-connected transistor are equal when said pre-charge signal is enabled and said target voltage is equal to VDD/2.

9. The pre-charge circuit as set forth in Claim 7 wherein said first and second diode-connected transistors are off when said pre-charge signal is disabled.

10. The pre-charge circuit as set forth in Claim 9 wherein said gate-biasing circuit holds said internal common node at said target voltage when said pre-charge circuit is disabled.

11. A signal generator comprising a phase-locked loop (PLL) circuit capable of generating an output reference signal having a desired frequency, said PLL circuit comprising:

a voltage-controlled oscillator;

a charge pump and loop filter circuit for generating a control voltage capable of controlling said voltage controlled oscillator; and

a pre-charge circuit capable of pre-charging said high-impedance node of said charge pump and loop filter to a target voltage when a pre-charge signal driving said pre-charge circuit is enabled, said pre-charge circuit comprising:

a charge voltage circuit capable of charging an internal common node of said pre-charge circuit to said target voltage when said pre-charge signal is enabled;

a transmission gate switch capable of coupling said internal node to said high-impedance node when said pre-charge signal is enabled, said transmission gate switch comprising a first N-channel transistor having a drain coupled to said high-impedance node, a gate coupled to a Logic 1 when said pre-charge signal is enabled, and a source coupled to said internal common node; and

a gate-biasing circuit driven by said pre-charge signal, wherein said gate-biasing circuit is off when said pre-charge signal is enabled and generates a negative Vgs bias on said first N-channel transistor when said pre-charge signal is disabled to thereby reduce leakage current in said first N-channel transistor.

12. The signal generator as set forth in Claim 11 wherein said transmission gate switch further comprises a first P-channel transistor having a drain coupled to said high-impedance node, a gate coupled to a Logic 0 when said pre-charge signal is enabled, and a source coupled to said internal common node.

13. The signal generator as set forth in Claim 12 wherein said gate-biasing circuit generates a positive Vgs bias on said first P-channel transistor when said pre-charge signal is disabled to thereby reduce leakage current in said first P-channel transistor.

14. The signal generator as set forth in Claim 13 wherein said gate of said first N-channel transistor is coupled to a Logic 0 when said pre-charge signal is disabled and said gate-biasing circuit holds said internal common node at a voltage higher than Logic 0 to thereby generate said negative Vgs bias on said first N-channel transistor when said pre-charge signal is disabled.

15. The signal generator as set forth in Claim 14 wherein said gate of said first P-channel transistor is coupled to a Logic 1 when said pre-charge signal is disabled and said gate-biasing circuit holds said internal common node at a voltage less than Logic 1 to thereby generate said positive Vgs bias on said first P-channel transistor when said pre-charge signal is disabled.

16. The signal generator as set forth in Claim 15 wherein said charge voltage circuit comprises a first diode-connected transistor and a second diode-connected transistor, wherein said first and second diode-connected transistors are connected as diodes in series between a VDD power supply rail and a ground rail when said pre-charge signal is enabled and wherein said internal common node is a connection node between said first and second diode-connected transistors.

17. The signal generator as set forth in Claim 16 wherein said target voltage is determined by an impedance of said first diode-connected transistor and an impedance of said second diode-connected transistor when said pre-charge signal is enabled.

18. The signal generator as set forth in Claim 17 wherein said impedance of said first diode-connected transistor and said impedance of said second diode-connected transistor are equal when said pre-charge signal is enabled and said target voltage is equal to VDD/2.

19. The signal generator as set forth in Claim 17 wherein said first and second diode-connected transistors are off when said pre-charge signal is disabled.

20. The signal generator as set forth in Claim 19 wherein said gate-biasing circuit holds said internal common node at said target voltage when said pre-charge circuit is disabled.